Remarks

Claims 1-22 have been canceled, claims 23 and 35 have been amended, and new claims 36-48 have been added. Claims 37-48 correspond to claims 24-35.

Claims 1-4, 6-8, 13, 16, and 23-35 were rejected as or unpatentable over KUDO et al. 6,853,037 in view of O 7,088,964 and the admitted prior art (APA). Reconsideration and withdrawal of the rejection are respectfully requested.

Amended claim 23 provides, among other features, that the MOS varactor film (the second insulating film) is thinner than the thinnest of the MOS transistor films (the first insulating films), where the MOS transistor films have a plurality of different thicknesses. Thus, the second insulating film is thinner than all the first insulating films. The references do not disclose this. In the references, the I/O transistor film thickness is greater than that of the logic film thickness, where the logic film thickness is the same as, not less than, the varactor film thickness. Accordingly, the claims avoid the rejection under §103.

KUDO discloses a semiconductor device with a plurality of MOS transistors having different gate insulating film thicknesses. O discloses that CMOS varactors are generally formed using design rules for logic devices and that logic devices are generally significantly smaller than I/O devices and use a thinner gate oxide (column 11, lines 17-21). The APA

acknowledges that logic devices and I/O devices are generally formed on the same chip.

Thus, the combination of these three references disclose that in a chip with logic devices and I/O devices, the thinnest gate insulating films among the MOS transistors is to be found in the logic devices. That is, the combination merely discloses that the gate insulating film of the varactors element is the same thickness as that of a gate insulating film of the thinnest MOS transistor on the chip. There is nothing in the combination that discloses that the thickness of the second gate insulating film in the varactor element is thinner than the thinnest gate insulating film among the first gate insulating films of the MOS transistors with different thicknesses.

New claim 36 provides, among other features, that the MOS varactor film (the second insulating film) is thinner than the thinnest of the MOS transistor films (the first insulating films), where the MOS transistor films all have a same thickness. Thus, the second insulating film is thinner than all the first insulating films. The references do not disclose this. In the references, the I/O transistor film thickness is greater than that of the logic film thickness, where the logic film thickness is the same as, not less than, the varactor film thickness. Accordingly, the new claims also avoid the rejection under §103.

In view of the foregoing remarks, it is believed that the present application is in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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